BASIC ELECTRONICS LAB MANUAL

EEC161/261

COURSE – B.TECH (CS)

Course Code: EEC261	B.Tech- Semester-II **Basic Electronics Engineering (Lab)**	L-0 T-0 P-2 C-1
Course Outcomes:	**On completion of the course, the students will be :**	
CO1.	**Understanding** the implementation of diode-based circuits.	
CO2.	**Understanding** the implementation of Operational amplifier-based circuits.	
CO3.	**Analyzing** the characteristics of pn junction diode & BJT.	
CO4.	**Analyzing** the different parameters for characterizing different circuits like rectifiers, regulators using diodes and BJTs.	
CO5.	**Analyzing** the truth tables through the different type's adders.	
LIST OF EXPERIMENTS:	**Note: Minimum eight experiments should be performed-**	
1	To study the V-I characteristics of p-n junction diode.	
2	To study the diode as clipper and clamper	
3	To study the half-wave rectifier using silicon diode.	
4	To study the full-wave rectifier using silicon diode.	
5	To study the Zener diode as a shunt regulator.	
6	To study transistor in Common Base configuration & plot its input/output characteristics	
7	To study the operational amplifier in inverting & non-inverting modes using IC 741.	
8	To study the operational amplifier as differentiator & integrator.	
9	To study various logic gates & verify their truth tables.	
10	To study half adder/full adder & verify their truth tables	

Evaluation Scheme of Practical Examination:

Internal Evaluation (50 marks)

Each experiment would be evaluated by the faculty concerned on the date of the experiment on a 4-point scale which would include the practical conducted by the students and a Viva taken by the faculty concerned. The marks shall be entered on the index sheet of the practical file.

Evaluation scheme:

PRACTICAL PERFORMANCE & VIVA DURING THE SEMESTER (35 MARKS)				ON THE DAY OF EXAM (15 MARKS)		TOTAL INTERNAL (50 MARKS)
EXPERIMENT (5 MARKS)	FILE WORK (10 MARKS)	VIVA (10 MARKS)	ATTENDANCE (10 MARKS)	EXPERIMENT (5 MARKS)	VIVA (10 MARKS)	

External Evaluation (50 marks)

The external evaluation would also be done by the external Examiner based on the experiment conducted during the examination.

EXPERIMENT (20 MARKS)	FILE WORK (10 MARKS)	VIVA (20 MARKS)	TOTAL EXTERNAL (50 MARKS)

Teerthanker Mahaveer University, Moradabad
Faculty of Engineering
Electronics & Communication Department
List of Equipmemts

Lab Name-Basic Electronics Lab (EEC161/EEC261)

Lab Technician-Mr. Pradeep Kumar

Stock Reg Page No.	Equipment	Quantity
1	Active Filters(Asico)- 1 item shifted to EDC	00
2	Adjustable Wrench (Hindustan Everest Tools Ltd.)	01
3	Common Base Transistor (Excel Tech)	02
4	Clipping & Clamping Circuit Apparatus(Mars)	02
5	Common Collector Transistor Amplifier(Asico) - 1 item shifted to EDC	00
6	FET Characteristics Apparatus (Mars) - 1 item shifted to EDC	00
7	Function Generator(Aplab)	01
8	Function Generator(Mars)	01
9	Foldable Industrial Soldering Iron (Silvertone trading Co.) 15W,25W	11
10	Half, Full Wave Rectifier Apparatus(Mars)	01
11	Half, Full Wave Rectifier Apparatus(Rajat)	01
12	h-parameter of PNP Transistor(Mars)	01
13	Junction Transistor as Amplifier and as Switch(Rajat)	01
14	Nose Plainer	01
15	Multimeter(Mastech-2,Mars-2)	07
16	Operational Amplifier(Asico)	01
17	Operational Amplifier as Differentiator and Integrator(Mars)	01
18	Op-Amp Trainer(Excel Tech)	01
19	C.R.O(Mars)	02
20	P N Junction Apparatus	01
21	Regulated DC Power Supply(Applab)	01
22	Dual Output Regulated Power Supply(Applab)	01
23	UJT Oscillator(Mars)	02
24	Zener Diode Apparatus	01
25	Tool Kit	01
26	Component (Transistor, Resistance, Diode, LED, Zener Diode etc.)	
27	Half Adder Kit(Mars)	01
28	Full Adder Kit(Mars)	01
29	PN Junction(Mars)	01
30	Characteristics of Transistor(Mars)	01
31	EDM-100 Desk Stand Meter 10V(OM)	20
32	EDM-100 Desk Stand Meter 5V(OM)	20
33	EDM-100 Desk Stand Meter 3V(OM)	25

34	EDM-100 Desk Stand Meter 5Amp(OM)	25
35	EDM-100 Desk Stand Meter 3Amp(OM)	15
36	EDM-100 Galvo Desk Stand Meter(OM)	05
37	Multimeter Analog	01
38	Multi Range A/V Meter	03
39	Portable Meter	05
40	Scale 10V DC	01
41	Scale 15V DC	01
42	Scale 5V DC	01
43	Scale 1Amp ac	01
44	Scale 15V ac	01
45	Scale 1Amp DC	01
46	Scale 500ma DC	01
47	Scale 500ma ac	01
48	Inter Scale Meter	01
49	C.R.O Scientech	03
50	Function Generator (Anshuman)	01
51	Components	

Teerthanker Mahaveer University
Faculty of Engineering
Department of Electronics and Communication

Subject Name-Basic Electronics Lab
Subject Code-EEC161/261

EXPERIMENT No.-1

OBJECT:-To study the V-I characteristics of p-n junction diode.

Equipment Used:-

S.No.	Name	Range	Qty
1	R.P.S	(0-30)V	1
2	Ammeter		1
3	Voltmeter		1

S.No.	Name	Range	Qty
1	Diode	IN4001	1
2	Resistor		1
4	Wires		

THEORY:-

A PN junction diode is a two terminal junction device. It conducts only in one direction (only on forward biasing).

FORWARD BIAS:-

On forward biasing, initially no current flows due to barrier potential. As the applied potential exceeds the barrier potential the charge carriers gain sufficient energy to cross the potential barrier and hence enter the other region. The holes, which are majority carriers in the P-region, become minority carriers on entering the N-regions, and electrons, which are the majority carriers in the N-region, become minority carriers on entering the P-region. This injection of Minority carriers results in the current flow, opposite to the direction of electron movement.

REVERSE BIAS:-

On reverse biasing, the majority charge carriers are attracted towards the terminals due to the applied potential resulting in the widening of the depletion region. Since the charge carriers are pushed towards the terminals no current flows in the device due to majority charge carriers. There will be some current in the device due to the thermally generated minority carriers. The generation of such carriers is independent of the applied potential and hence the current is constant for all increasing reverse potential. This current is referred to as Reverse Saturation Current (I_O) and it increases with temperature. When the applied reverse voltage is increased beyond the certain limit, it results in breakdown. During breakdown, the diode current increases tremendously.

RESULT:-

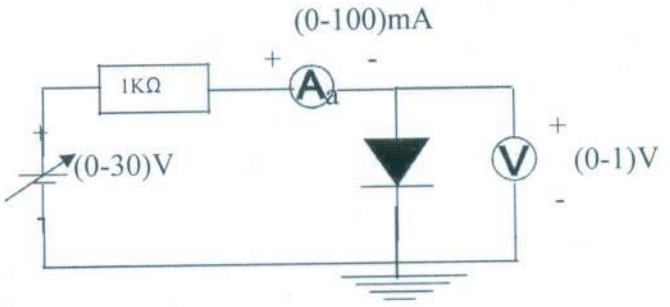
Forward and Reverse bias characteristics of the PN junction diode was Studied

PRECAUTIONS:-

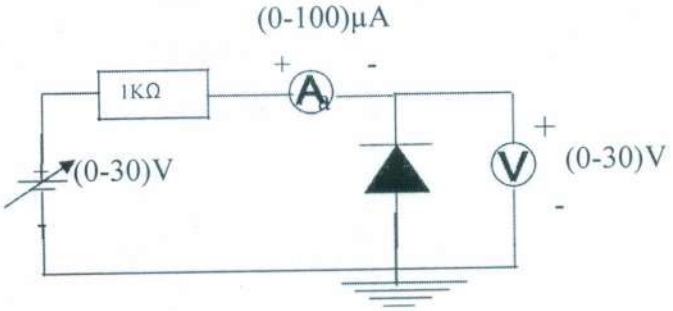
1. All connections should be right & tight.
2. Do not touch any live wires.
3. Reading should be taken carefully.

CIRCUIT DIAGRAM:-

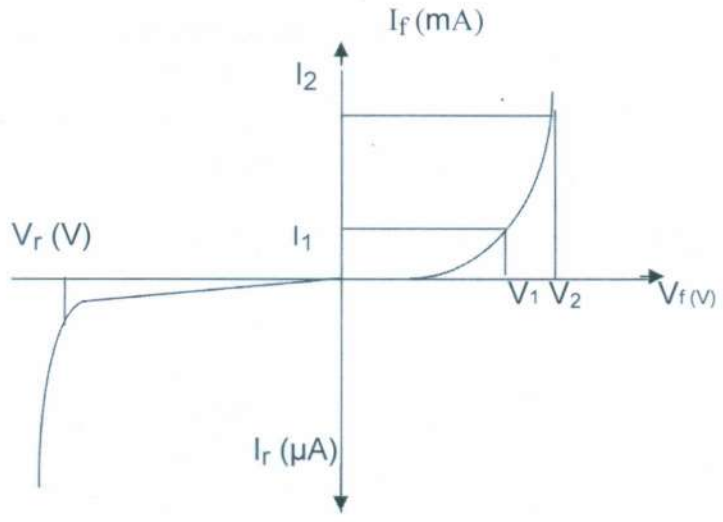
FORWARD BIAS:-



REVERSE BIAS:-



MODEL GRAPH:-



Observation Table:-

FORWARD BIAS **REVERSE BIAS**

S.No.	VOLTAGE(V_f) (In Volts)	CURRENT(I_f) (In mA)	S..No.	VOLTAGE(V_r) (In Volts)	CURRENT(I_r) (In μA)

Teerthanker Mahaveer University
Faculty of Engineering
Department of Electronics and Communication

Subject Name-Basic Electronics Lab
Subject Code-EEC161/261

EXPERIMENT No-2

OBJECT: To Study the diode as clipper & clamper.

CLIPPER

Equipment Used:

S.NO.	Name of the Apparatus	Range	Quantity
1	Resistor	3.3 KΩ	1
2	DC source	3 V	1
3	Diode	IN4007	1
4	CRO	-	1
5	Function Generator	-	1

THEORY:

Clipping circuits are non-linear wave shaping circuits. They are useful to clip off the positive or negative portions of an input waveform. It can be also used to slice off an input waveform between two voltage levels. The diode clippers can be classified as series and shunt clippers. The property of a diode as a switching device is utilized in clipping circuits. In the shunt clippers, output is taken parallel with the diode and in series clippers, output is taken in series with the diode. In other words, in the shunt clippers (parallel clippers), load comes in parallel with the diode and in series clippers, load comes in series with the diode.

Positive clipper clipping at 0 V: This circuit passes only negative going half waves of the input to the output. All the positive half cycles are bypassed through the diode to ground terminal because the diode gets forward biased when the input voltage becomes positive. Due to the voltage drop across the diode, the clipping occurs at +0.6 V.

Negative clipper clipping at 0 V: This circuit passes only positive going half waves of the input to the output. All the negative half cycles are bypassed through the diode to ground terminal because the diode gets forward biased when the input

voltage becomes negative. Due to the voltage drop across the diode, the clipping occurs at -0.6 V.

Positive clipper clipping at + 3V: Till the input becomes greater than + 3 V, diode is reverse biased and the input appears at the output. When input is greater than +3V, diode becomes forward biased and cell voltage appears at the output. Since the voltage drop across the diode develops in series with the cell, actual clipping level is at +3.6 V.

Positive clipper clipping at – 3V: Diode becomes reverse biased when the input voltage is less than – 3V and the input appears at the output. When the input is above – 3V, diode becomes forward biased and the cell voltage is available at the output since the voltage drop across the diode develops in series and opposite with the cell, actual clipping level is at – 2.4 V.

Negative clipper clipping at – 3V: When the input voltage becomes less than -3 V, diode becomes forward biased and the cell voltage becomes available at the output. When the input is greater than – 3 V, diode is reverse biased and the input appears at the output. Actual clipping level is at – 3.6 V, due to the voltage drop across the diode.

Negative clipper clipping at + 3V: Diode becomes reverse biased when the input voltage is greater than + 3V and the input appears at the output. When the input is below + 3V, diode becomes forward biased and the cell voltage is available at the output since the voltage drop across the diode develops in series and opposite with the cell, actual clipping level is at + 2.4 V.

Double clipper clipping at + 3V & - 3 V: This circuit is the combination of positive and negative clippers. During the positive half cycle of the input, one branch is effective and the other remains open &vice versa during the negative half cycle. Actual clipping levels are + 3.6 V & - 3.6 V due to the diode drops.

Slicer: A slicer circuit is nothing but a two level clipper which has both clipping levels either in the positive or in negative part of the input signal. Consider the two level slicer with slicing levels at + 3V and +5V. This circuit allows the input signal pass to the output only between +3V & +5V. During the negative half cycle of the input, diode D_1 conducts & diode D_2 get reverse biased. The output voltage remains at +3V because the diode D_1 conducts when the input is less than +3V. During the positive half cycle of the input when input exceeds +3V, D_1 is reverse biased and input appears at the output. If the input exceeds +5 V, D_2 conducts and the output remain at +5 V. When the diode drop is considered, actual clipping occurs at +2.4 V & +5.6 V.

Unbiased positive clipper: This circuit passes only negative going half waves of the input to the output. During the positive going half cycle of the input, diode turns off. Since 0.6V get dropped across the diode during conduction, amplitude of the output peak is reduced by 0.6 V.

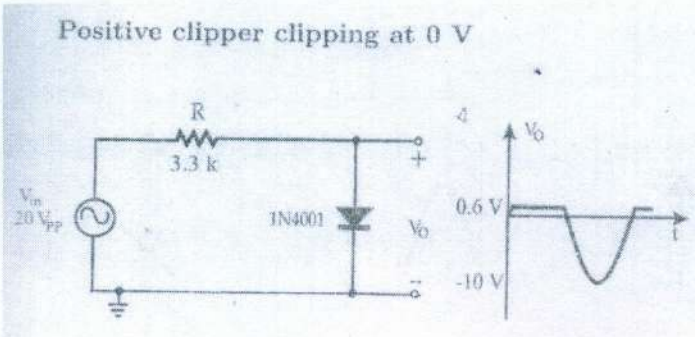
Unbiased negative clipper: This circuit passes only positive going half waves of the input to the output. During the negative going half cycle of the input, diode turns off. Amplitude of the output peak is reduced by 0.6 V.

Biased clippers: Diodes in the positive and negative clippers are either forward biased or reverse biased in these circuits. Thus four combinations of diodes and dc sources create four different clipping circuits namely, forward biased positive clipper, reverse biased positive clipper, forward biased negative clipper and reverse biased negative clipper. When the dc source is connected such a way that it reverse biases the diode, the peak value of the output voltage is smaller than the input peak value by the amount of the dc voltage applied. Diode conducts only when the input voltage sufficiently high to forward bias the diode. When the dc source is connected such a way that it forward biases the diode, the peak value of the output voltage is greater than the input peak by the amount of the dc voltage applied.

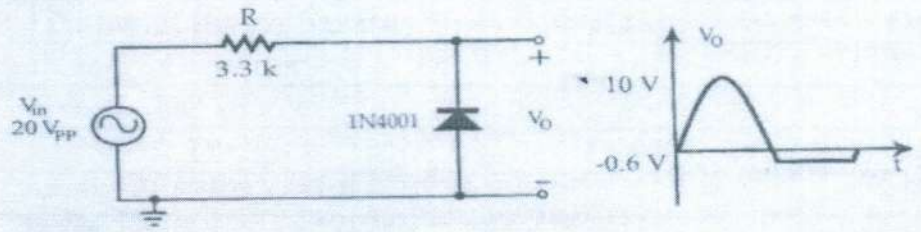
PROCEDURE:

1. Set up the circuit one by one after testing the components. Apply 20V peak to peak sine at the input.
2. Observe the input & output waveforms simultaneously on the CRO screen.
3. Note the values & plot the waveform.

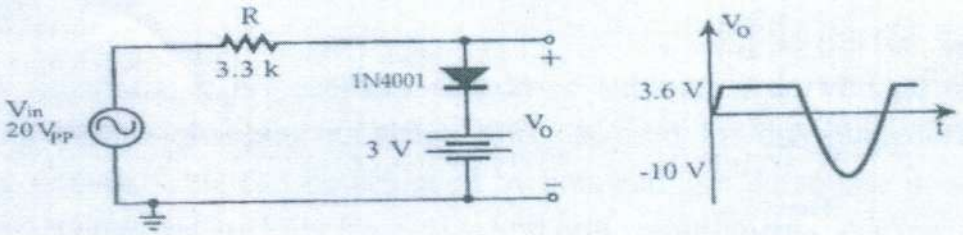
Circuit Diagrams & Model Waveforms:



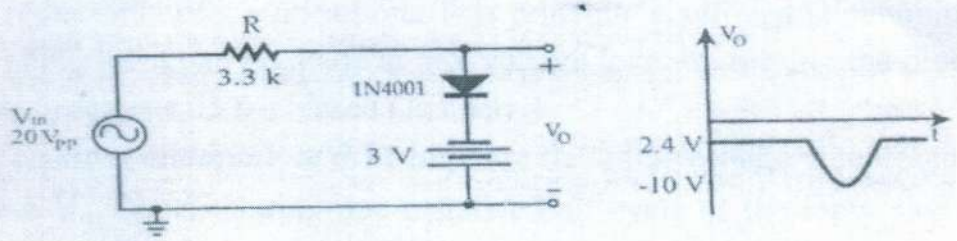
Negative clipper clipping at 0 V



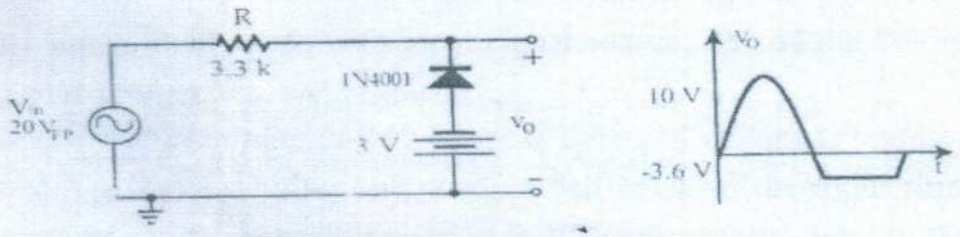
Positive clipper clipping at +3 V



Positive clipper clipping at -3 V



Negative clipper clipping at -3 V



Result-

CLAMPER

Equipment Used:

S.NO.	Name of the Apparatus	Range	Quantity
1	Capacitor	1μF	1
2	DC source	3 V	1
3	Diode	1N4007	1
4	CRO	-	1
5	Function Generator	-	1

THEORY:

In some situations, it is necessary to add or subtract a dc voltage to a given waveform without changing its shape. Circuits used for this purpose are called clamping circuits. This can be achieved by connecting a dc source in series with the input. DC sources are very expensive and bulky equipments. A capacitor which is charged to a voltage & subsequently prevented from discharging can serve as a suitable replacement for a dc source. This principle is utilized in clamping circuits. The clamping level can be made at any voltage level by biasing the diode. Such a clamping circuit is called a biased clamper.

Positive clamper clamping at 0 V: Suppose the input voltage is represented by the expression V_m Sinωt. During one negative half cycle of the input sine wave, the diode conducts and the capacitor charges to V_m with positive polarity at the right side of the capacitor. During the positive half of the input sine wave, the capacitor cannot discharge since the diode does not conduct. Thus capacitor acts as a dc source of V_m volts in series with input signal source. The output voltage then can be expressed as $V_o = V_m + V_m$ Sinωt

Negative clamper clamping at 0 V: Suppose the input voltage is represented by the expression V_m Sinωt. During one positive half cycle of the input sine wave, the diode conducts and the capacitor charges to V_m with positive polarity at the right side of the capacitor. During the positive half of the input sine wave, the capacitor cannot discharge since the diode does not conduct. Thus capacitor acts as a dc source of V_m volts in series with input signal source. The output voltage then can be expressed as $V_o = - V_m + V_m$ Sinωt

Positive clamper clamping at + 3V: During one negative half cycle of the input sine wave, capacitor charges through the dc source and diode till (V_m + 3) volts with

positive polarity of the capacitor at its right side. The charging of the capacitor is limited to (V_m + 3) volts due to the presence of the dc source. The output is then expressed as $V_o = (V_m + 3) + V_m \text{Sin}\omega t$

Positive clamper clamping at – 3V: During one negative half cycle of the input sine wave, capacitor charges through the dc source and diode till (V_m - 3) volts with positive polarity of the capacitor at its right side. The charging of the capacitor is limited to (V_m - 3) volts due to the presence of the dc source. The output is then expressed as $V_o = (V_m - 3) + V_m \text{Sin}\omega t$

Negative clamper clamping at + 3V: During one positive half cycle of the input sine wave, capacitor charges through the dc source and diode till (V_m - 3) volts with negative polarity of the capacitor at its right side. The charging of the capacitor is limited to (V_m - 3) volts due to the presence of the dc source. The output is then expressed as $V_o = -(V_m - 3) + V_m \text{Sin}\omega t$

Negative clamper clamping at - 3V: During one positive half cycle of the input sine wave, capacitor charges through the dc source and diode till (V_m + 3) volts with negative polarity of the capacitor at its right side. The charging of the capacitor is limited to (V_m + 3) volts due to the presence of the dc source. The output is then expressed as $V_o = -(V_m + 3) + V_m \text{Sin}\omega t$.

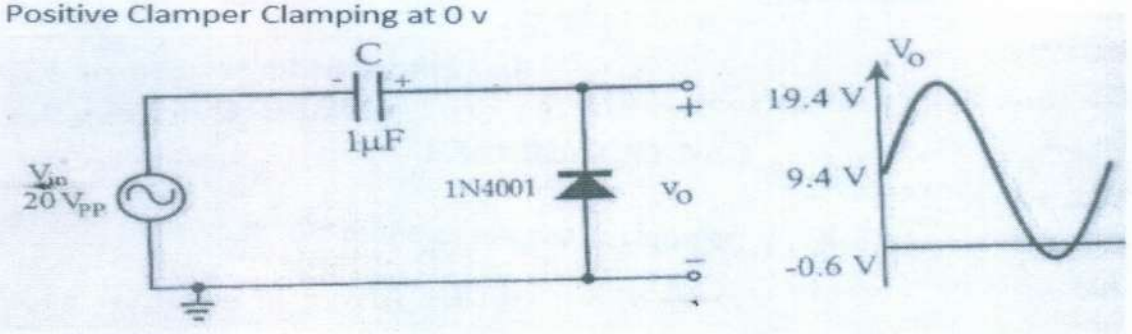
Note in the above discussion the voltage drop across the diode is neglected to simplify the discussion. Voltage across the diode (0.6 V) is not negligible compared to clamping voltage of 3 V. Therefore, it must be considered.

PROCEDURE:

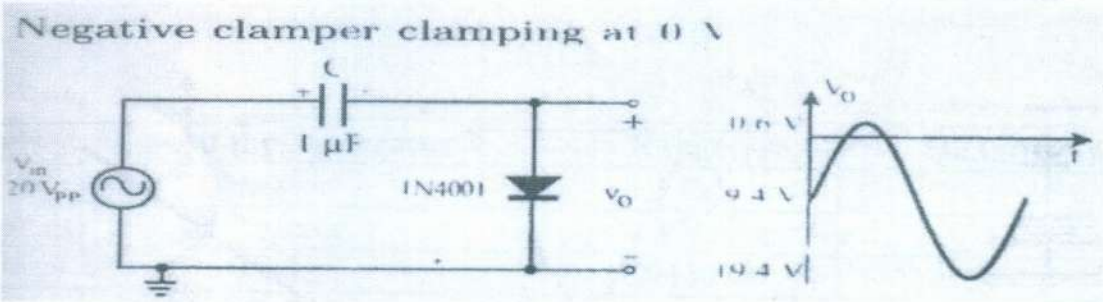
1. Set up the circuit one by one after testing the components. Apply 20V peak to peak sine at the input.
2. Observe the input & output waveforms simultaneously on the CRO screen keeping AC-DC switch of the CRO in DC position.
3. Note the values & plot the waveform.

Circuit Diagrams & Model Waveforms:

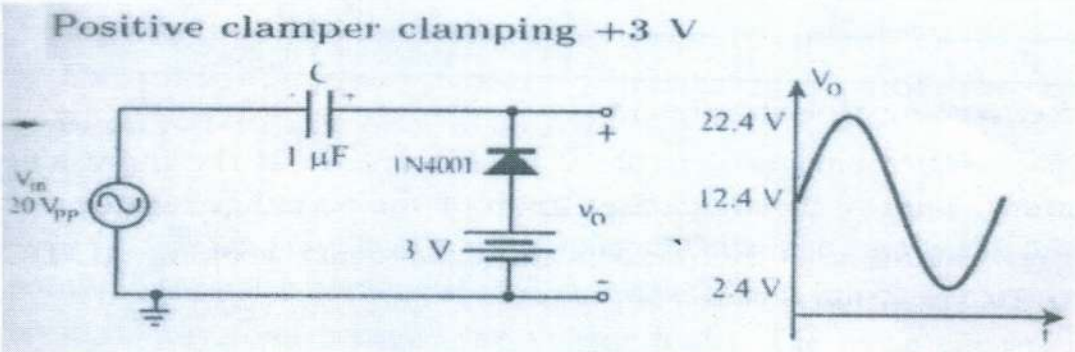
Positive Clamper Clamping at 0 v



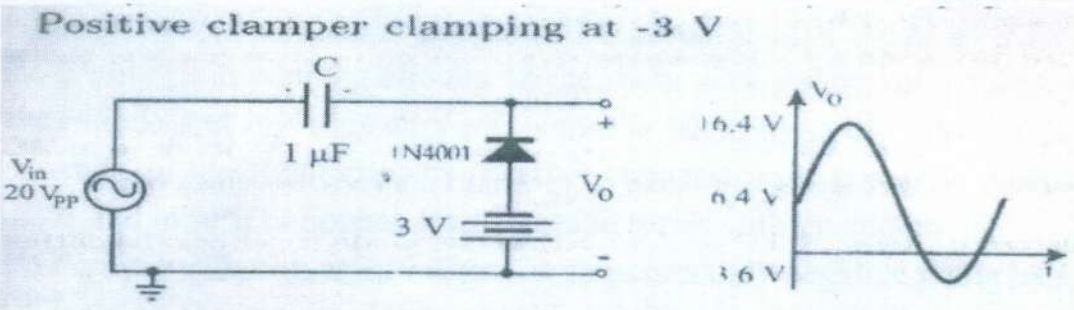
Negative clamper clamping at 0 V



Positive clamper clamping +3 V



Positive clamper clamping at -3 V



Result-

PRECAUTIONS:-

1. All connections should be right & tight.
2. Do not touch any live wires.

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Faculty of Engineering
Department of Electronics and Communication

Subject Name-Basic Electronics Lab
Subject Code-EEC161/261

EXPERIMENT No-3

Object:

To study the Half-wave rectifier using silicon diode.

Equipment Used:

S.NO.	Name of the Apparatus	Range	Quantity
1	Resistor	1 KΩ	1
2	Diode	1N4007	1
3	CRO	-	1

THEORY:

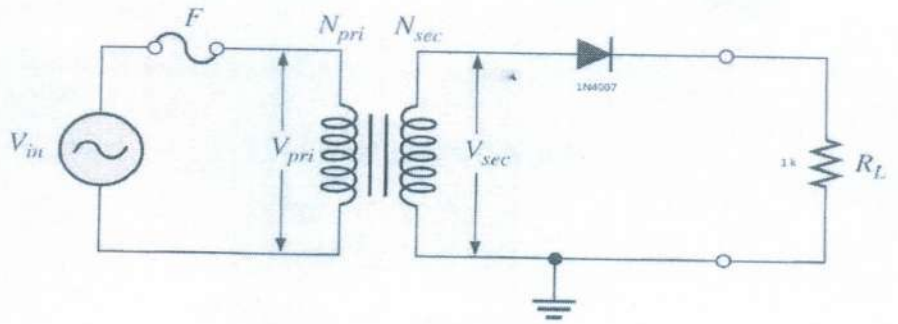
Rectifier changes ac to dc and it is an essential part of a power supply. The unique property of a diode, permitting the current to flow in one direction, is utilized in rectifiers.

HALF WAVE RECTIFIER: Mains power supply is applied at the primary of the step down transformer. All the positive half cycles of the stepped down ac supply pass through the diode and all the negative half cycles get eliminated. Peak value of the output voltage is less than the peak value of the input voltage by 0.6 V because of the voltage drop across the diode.

For a half wave rectifier, $V_{rms} = V_m/2$ and $V_{dc} = V_m/\pi$ where V_{rms} = *rms* value of the input, V_{dc} = Average value of input and V_m = peak value of the output. The ripple factor $r = V_{r,rms}/ V_{dc}$ where $V_{r,rms}$ is the rms value of the ac component. $r = \{(V_{rms}/ V_{dc})^2 - 1\}^{1/2} = 1.21$

PROCEDURE:

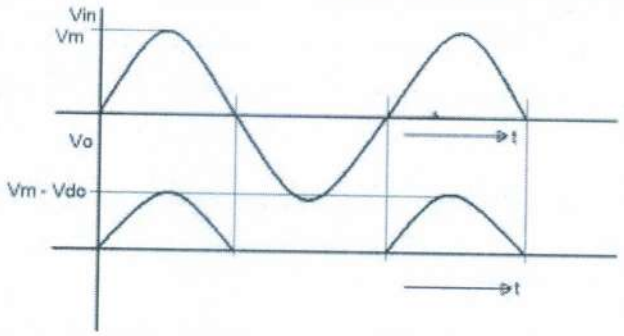
1. Switch on mains supply. Observe the transformer secondary voltage waveform and output voltage waveform across the load resistor, simultaneously on the CRO screen. Note down V_m & calculate V_{rms} & V_{dc}
2. Calculate the ripple factor using the expression and plot the waveform.



Figure

Model Graph:

Half Wave Rectifier: V_{do} stands for voltage drop across the diode.



Result

PRECAUTIONS:-

1. All connections should be right & tight.
2. Do not touch any live wires.

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EXPERIMENT No-4

Object:

To study the full-wave rectifier using silicon diode.

Equipment Used:

S.NO.	Name of the Apparatus	Range	Quantity
1	Resistor	1 KΩ	1
2	Diode	1N4007	1
3	CRO	-	1

THEORY:

Rectifier changes ac to dc and it is an essential part of a power supply. The unique property of a diode, permitting the current to flow in one direction, is utilized in rectifiers.

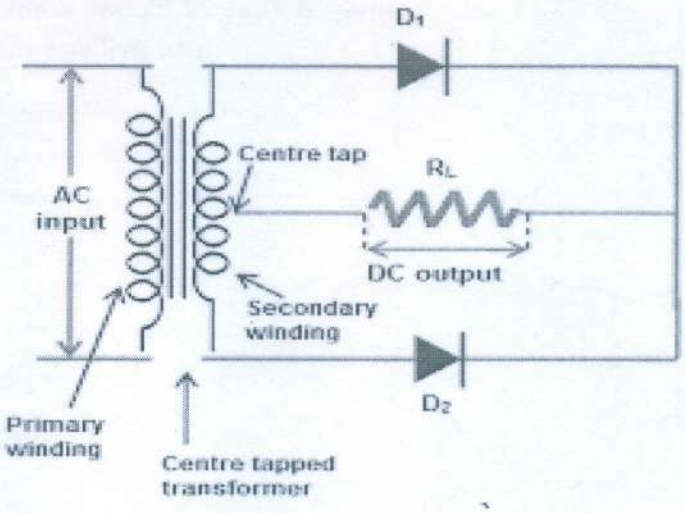
FULL WAVE RECTIFIER: During the positive half cycle of the transformer secondary voltage, diode D_1 is forward biased and D_2 is reversed biased. So a current flows through the diode D_1, load resistor R_L and upper half of the transformer winding. During the negative half cycle, diode D_2 becomes forward biased and D_1 becomes reverse biased. The current then flows through the diode D_2, load resistor R_L and lower half of the transformer winding. Current flows through the load resistor in the same direction during both the half cycles. Peak value of the output voltage is less than the peak value of the input voltage by 0.6 V because of the voltage drop across the diode.

For a full wave rectifier, $V_{rms} = V_m/1.414$, $V_{dc} = 2V_m/\pi$.

Ripple factor $r = \{(V_{rms}/V_{dc})^2 - 1\}^{1/2} = 0.48$

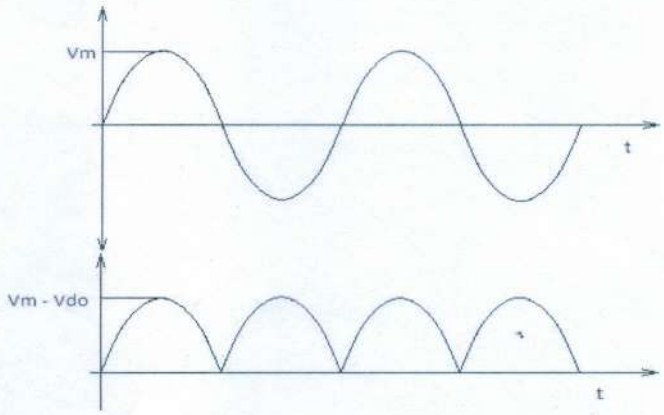
PROCEDURE:

1. Switch on mains supply. Observe the transformer secondary voltage waveform and output voltage waveform across the load resistor, simultaneously on the CRO screen. Note down V_m & calculate V_{rms} & V_{dc}
2. Calculate the ripple factor using the expression and plot the waveform.



Model Graph:

Full Wave Rectifier: V_{do} stands for voltage drop across the diode.



Tabulation:

Table 1:

	V_m (v)	V_{rms} (v)	V_{dc} (v)	Ripple Factor *r*
Half Wave Rectifier				

Result-

PRECAUTIONS:-

1. All connections should be right & tight.
2. Do not touch any live wire.

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EXPERIMENT No-5

OBJECT: To study the zener diode as a shunt regulator

Equipment Used: 1 Zener Diode

2 Resistances

3. Ammeter & Voltmeter

Theory:

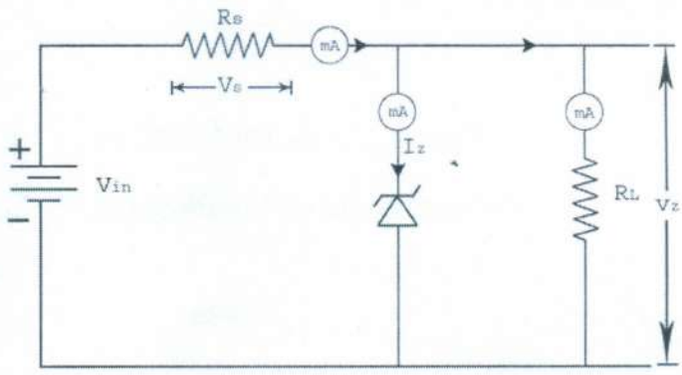
The function of a regulator is to provide a constant output voltage to a load connected in parallel with it in spite of the ripples in the supply voltage or the variation in the load current and the zener diode will continue to regulate the voltage until the diodes current falls below the minimum $I_{Z\,(min)}$ value in the reverse breakdown region. It permits current to flow in the forward direction as normal, but will also allow it to flow in the reverse direction when the voltage is above a certain value - the breakdown voltage known as the zener voltage. The zener diode specially made to have a reverse voltage breakdown at a specific voltage. Its characteristics are otherwise very similar to common diodes. In breakdown the voltage across the zener diode is close to constant over a wide range of currents thus making it useful as a shunt voltage regulator.

The purpose of a voltage regulator is to maintain a constant voltage across a load regardless of variations in the applied input voltage and variations in the load current. A typical zener diode shunt regulator is shown in Figure 3. The resistor is selected so that when the input voltage is at $V_{IN\,(min)}$ and the load current is at $I_{L\,(max)}$ that the current through the zener diode is at least $I_{z(min)}$. Then for all other combinations of input voltage and load current the zener diode conducts the excess current thus maintaining a constant voltage across the load. The zener conducts the

least current when the load current is the highest and it conducts the most current when the load current is the lowest.

If there is no load resistance, shunt regulators can be used to dissipate total power through the series resistance and the zener diode. Shunt regulators have an inherent current limiting advantage under load fault conditions because the series resistor limits excess current.

A zener diode of break down voltage V_z is reverse connected to an input voltage source V_i across a load resistance R_L and a series resistor R_S. The voltage across the zener will remain steady at its break down voltage V_Z for all the values of zener current I_Z as long as the current remains in the break down region. Hence a regulated DC output voltage $V_0 = V_Z$ is obtained across RL, whenever the input voltage remains within a minimum and maximum voltage.



PROCEDURE:

(a)Connect the circuit as per the circuit diagram
(b)Keep load resistance constant (take maximum value of load resistance)
(c)Vary input voltage and note down output voltage
(d)Now keep input voltage constant and vary load resistance and note down corresponding voltmeter reading
(e)Plot the respective graph

OBSERVATION TABLE:

S.No	Input Voltage	Output Voltage

RESULT: Plot the graph between input voltage & output voltage.

Precautions: 1-All connections should be tight

2-Reading should be taken carefully.

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Faculty of Engineering
Department of Electronics and Communication

Subject Name-Basic Electronics Lab
Subject Code-EEC161/261

EXPERIMENT No-6

OBJECT: To study transistor in common base configuration & plot input/output characteristics

Equipment Used:

S.No.	Name	Range	Type	Qty
1	R.P.S	(0-30)V		2
2	Ammeter	(0–10)mA		1
		(0–1)A		1
3	Voltmeter	(0–30)V		1
		(0–2)V		1

S.No.	Name	Range	Type	Qty
1	Transistor	BC 107		1
2	Resistor	10kΩ 1KΩ		1
3	Bread Board			1
4	Wires			

THEORY:

In this configuration the base is made common to both the input and out. The emitter is given the input and the output is taken across the collector. The current gain of this configuration is less than unity. The voltage gain of CB configuration is high. Due to the high voltage gain, the power gain is also high. In CB configuration, Base is common to both input and output. In CB configuration the input characteristics relate I_E and V_{EB} for a constant V_{CB}. Initially let V_{CB} = 0 then the input junction is equivalent to a forward biased diode and the characteristics resembles that of a diode. Where $V_{CB} = +V_I$ (volts) due to early effect I_E increases and so the characteristics shifts to the left. The output characteristics relate I_C and V_{CB} for a constant I_E. Initially I_C increases and then it levels for a value $I_C = \alpha I_E$. When I_E is increased I_C also increases proportionality. Though increase in

V_{CB} causes an increase in α, since α is a fraction, it is negligible and so I_C remains a constant for all values of V_{CB} once it levels off.

PROCEDURE:

INPUT CHARACTERISTICS:

It is the curve between emitter current I_E and emitter-base voltage V_{BE} at constant collector-base voltage V_{CB}.

1. Connect the circuit as per the circuit diagram.
2. Set V_{CE}=5V, vary V_{BE} in steps of 0.1V and note down the corresponding I_B. Repeat the above procedure for 10V, 15V.
3. Plot the graph V_{BE} Vs I_B for a constant V_{CE}.
4. Find the h parameters.

OUTPUT CHARACTERISTICS:

It is the curve between collector current I_C and collector-base voltage V_{CB} at constant emitter current I_E.

1. Connect the circuit as per the circuit diagram.
2. Set I_B=20μA, vary V_{CE} in steps of 1V and note down the corresponding I_C. Repeat the above procedure for 40μA, 80μA, etc.
3. Plot the graph V_{CE} Vs I_C for a constant I_B.
4. Find the h parameters

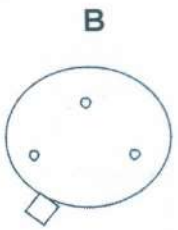
RESULT:

The transistor characteristics of a Common Base (CB) configuration were plotted and studied.

PRECAUTIONS:-

1. All connections should be right & tight.
2. Do not touch any live wires.
3. Reading should be taken carefully.

PIN DIAGRAM:

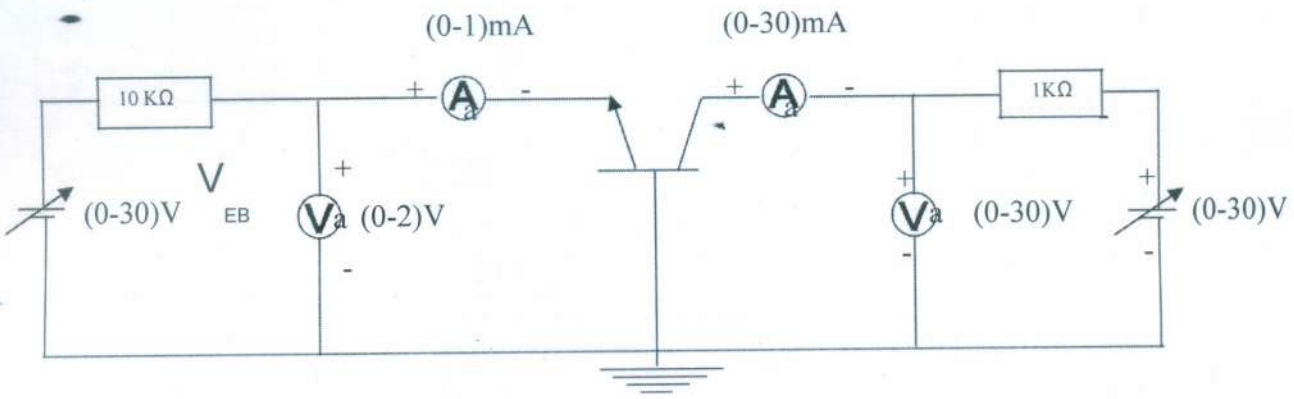


Bottom View

BC107

Specification: BC107/50V/0.1A,0.3W,300MHz

CIRCUIT DIAGRAM:



OBSERVATION TABLE:

INPUT CHARACTERISTICS:

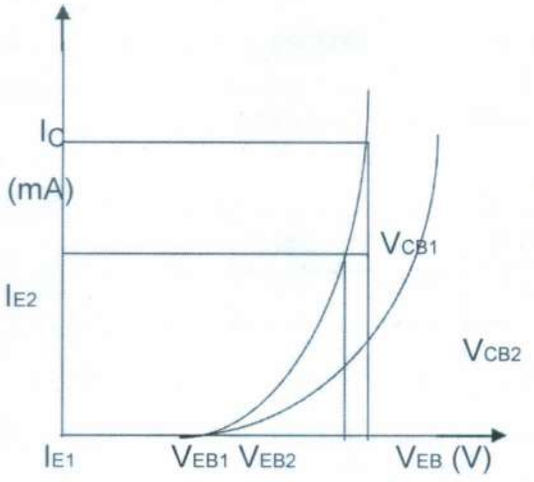
S.No.	V_{CB} = V		V_{CB} = V		V_{CB} = V	
	V_{EB} (V)	I_E (μA)	V_{EB} (V)	I_E (μA)	V_{EB} (V)	I_E (μA)

OUTPUT CHARACTERISTICS:

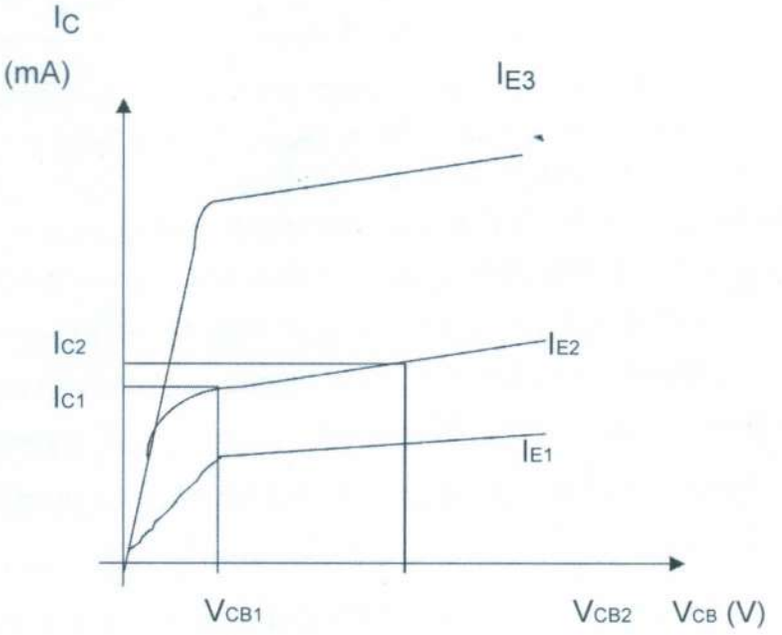
S.No.	I_E= mA		I_E= mA		I_E= mA	
	V_{CB} (V)	Ic (mA)	V_{CB} (V)	Ic (mA)	V_{CB} (V)	Ic (mA)

MODEL GRAPH:

INPUT CHARACTERISTICS:



OUTPUT CHARACTERISTICS:



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Department of Electronics and Communication

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Subject Code- EEC 161/261

EXPERIMENT No-7

Object- To study the operational amplifier in inverting and non inverting modes using IC 741.

Equipment Used- : Op – Amp IC 741 Dual Power Supply 15V, Resistors, Capacitors, Function Generator,Cathode Ray Oscilloscope, Multimeter

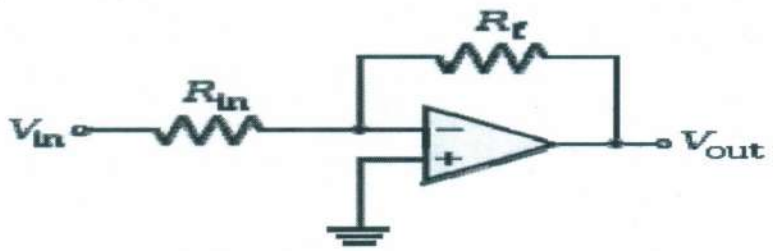
Theory-

Inverting Amplifier: This is the most widely used of all the Op-amp circuits. The output V0 is fed back to the inverting input through the Rf in network as shown in figure where Rf is the feedback resistor. The input signal Vi is applied to the inverting input terminal through Rin and non-inverting input terminal of Op-amp is grounded.The output V0 is given by

$$V0 = Vi\ (-Rf / Rin)$$

Where, the gain of amplifier is - Rf / Rin .The negative sign indicates a phase-shift of 180 degrees between Vi and V0. The effective input impedance is Ri. An inverting amplifier uses negative feedback to invert and amplify a voltage. The Rf resistor network allows some of the output signal to be returned to the input. Since the output is 180° out of phase, this amount is effectively subtracted from the input, thereby reducing the input into the operational amplifier. This reduces the overall gain of the amplifier and is dubbed negative feedback

Circuit Diagram:



Non – inverting amplifier : The circuit diagram of non inverting amplifier is shown ion figure. The signal is applied to the non-inverting input terminal and feedback is given to inverting terminal. The circuit amplifiers the input signal without inverting it. The output Vout is given by

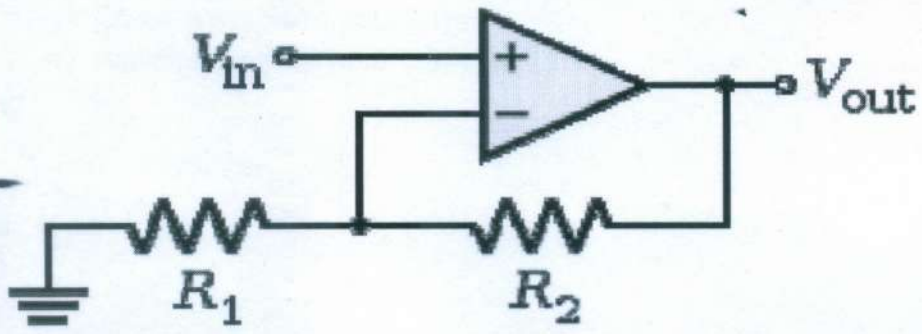
Vout = Vin (1+R2/R1)

The voltage gain is given by

$$A_{CL} = \frac{V_{Out}}{Vin} = \left[1 + \frac{R_2}{R_1}\right]$$

Compared to the inverting amplifier, the inpuut resistancee of the non-iinverting is eextremely laarge.

Circuit Diagram:



Observation Table-

Table for Inverting Mode

S.No	Input	Output

Table for Non- Inverting Mode

S.No	Input	Output

Result- Thus the linear applications of 741 op amp were studied experimentally.

Precautions-

1) Connection Should be right and tight.
2) Donot touch linewire.
3) Trace waveform carefully.
4) Reading should be taken carefully.

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EXPERIMENT No-8

Object- To Study the operational amplifier as differentiator & integrator.

Equipment Used-CRO,Connecting Leads,Kit

Theory-

In this laboratory experiment, you will learn several basic ways in which an op-amp can be connected using *–ve feedback* to *stabilize the gain* and increase the *frequency response*. The extremely high *open-loop gain* of an op-amp creates an unstable situation because a small noise voltage on the input can be amplified to a point where the amplifier in driven out of its linear region. Also unwanted oscillations can occur. In addition, the open-loop gain parameter of an op-amp can vary greatly from one device to the next. Negative feedback takes a portion of output and applies it back out of phase with the input, creating an effective reduction in gain. This *closed-loop gain* is usually much less than the open-loop gain and independent of it.

Differentiator: An op-amp differentiator simulates mathematical differentiation, which is a process of determining the instantaneous rate of change of a function. Differentiator performs the reverse of integration function. The output waveform is derivative of the input waveform. Here, the input element is a capacitor and the feedback element is a resistor. An ideal differentiation is shown in fig.

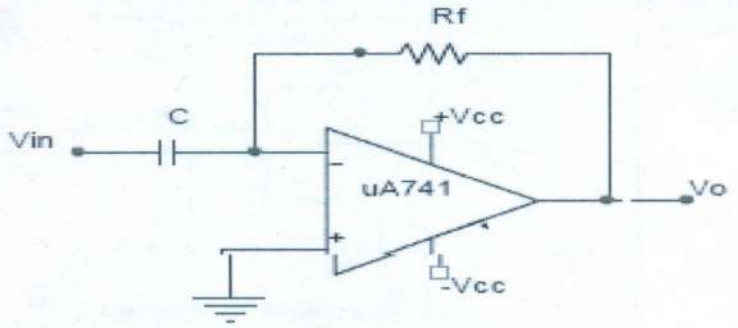
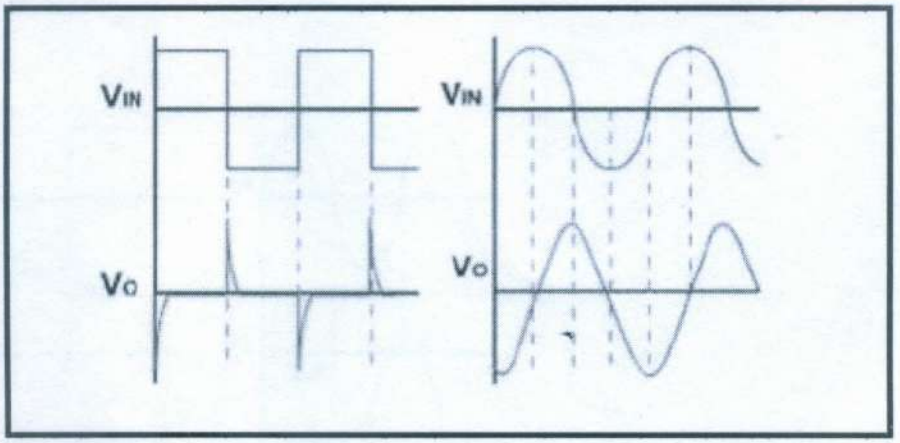


Fig Basic op-amp differentiator



The output voltage is given by

$$V_O = -RC\left(\frac{dV_S}{dt}\right)$$

Integrator

A circuit in which the output waveform is the integral of the input wave is the integrator. Such a circuit is obtained by using a basic inverting amplifier configuration. If the feedback resistor Rf is replaced by a capacitor C. The output voltage can be obtained by,

Vo= -1/RCf ∫ Vin dt+C

Where C is the integration constant and proportional to the value of the output voltage Vo at time t=0 sec. Thus, the output voltage is directly proportional to the negative integral of the input voltage and inversely proportional to the time constant R Cf.

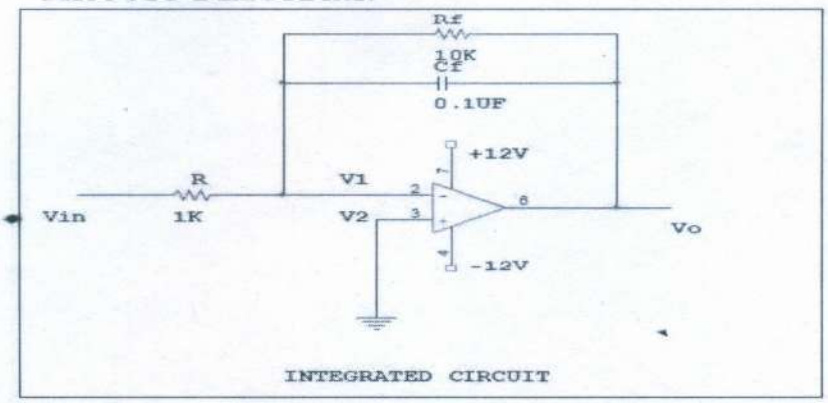
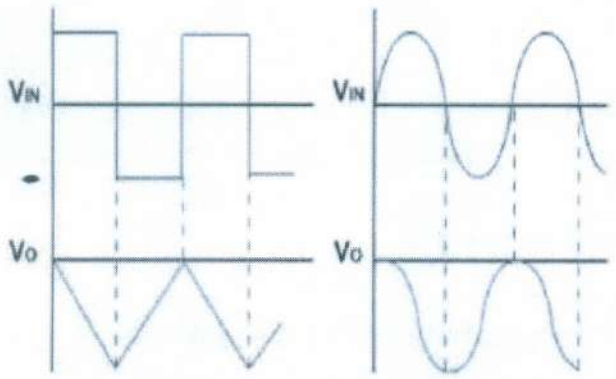


Fig Basic op-amp integrator

GRAPH:-



Result: Operational amplifier as integrator and differentiator has been studied.

Precautions:

1. All the steps should be followed and circuit diagram should be correct.
2. Observe the result carefully.
3. System should be switched off after use.

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EXPERIMENT No-9

Object: To study various logic gates & verify their truth tables.

Equipment Used: Power Supply, Digital Trainer Kit, Connecting Lead (7400, 7402, 7404, 7432, 7408, 7486)

THEORY:

NAND GATE: The IC no. for NAND gate is 7400. The NOT-AND operation is known as NAND operation. If all inputs are 1 then output produced is 0. NAND gate is inverted AND gate.

NAND  $F = (xy)'$

x	y	F
0	0	1
0	1	1
1	0	1
1	1	0

NOR GATE: The NOR gate has two or more input signals but only one output signal. IC 7402 is two I/P IC. The NOT- OR operation is known as NOR operation. If all the inputs are
0 then the O/P is 1. NOR gate is inverted OR gate.

NOR  $F = (x + y)'$

x	y	F
0	0	1
0	1	0
1	0	0
1	1	0

EX-OR GATE: The EX-OR gate can have two or more inputs but produce one output. 7486 is two input IC. EX-OR gate is not a basic operation & can be performed using basic gates.

Exclusive-OR (XOR)

$F = xy' + x'y$
$= x \oplus y$

x	y	F
0	0	0
0	1	1
1	0	1
1	1	0

AND GATE The AND operation is defined as the output as one if and only if all the inputs are one. 7408 is the two Inputs AND gate IC.A&B are the Input Terminals &Y is the Output terminal.

AND

$F = xy$

x	y	F
0	0	0
0	1	0
1	0	0
1	1	1

OR Gate: The OR operation is defined as the output as one if one or more than one inputs are one. 7432 is the two Input OR gate IC. A&B are the input terminals & Y is the Output terminal.

Y = A + B

OR

$F = x + y$

x	y	F
0	0	0
0	1	1
1	0	1
1	1	1

NOT GATE: The NOT gate is also known as Inverter. It has one input (A) & one output (Y). IC No. is 7404. Its logical equation is,

Inverter

$F = x'$

x	F
0	1
1	0

PROCEDURE:

(a) Fix the IC's on breadboard & give the input supply.
(b) Connect the +ve terminal of supply to pin 14 & -ve to pin 7.
(c) Give input at pin 1, 2 & take output from pin 3. It is same for all except NOT & NOR IC.
(d) For NOR, pin 1 is output & pin 2&3 are inputs.
(e) For NOT, pin 1 is input & pin 2 is output.
(f) Note the values of output for different combination of inputs & draw the TRUTH TABLE.

OBSERVATION TABLE:

AND		OR		NOT		NOR		NAND		EX-OR	
I/P	O/P	I/P	O/P	I/P	O/P	I/P	O/P	I/P	O/P	I/P	O/P

RESULT: We have learnt all the gates ICs according to the IC pin diagram.

PRECAUTIONS:

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.

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EXPERIMENT No-10

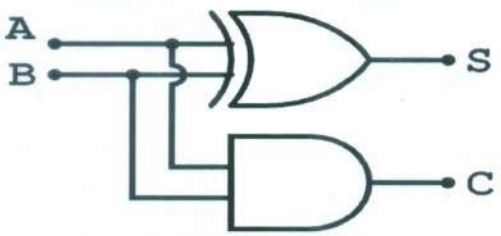
OBJECT: To study half adder/full adder & verify their truth tables.

Equipment Used:

- DC Power Supply 5V Battery
- Light Emitting Diode (LED)
- Digital ICs: 7408 :Quad 2 input AND
  7486: Quad 2 input EXOR
  7432: Quad 2 input OR

Theory:

Half Adder: A half adder is a logical circuit that performs an addition operation on two binary digits. The half adder produces a sum and a carry value which are both binary digits.



Circuit Diagram of Half Adder

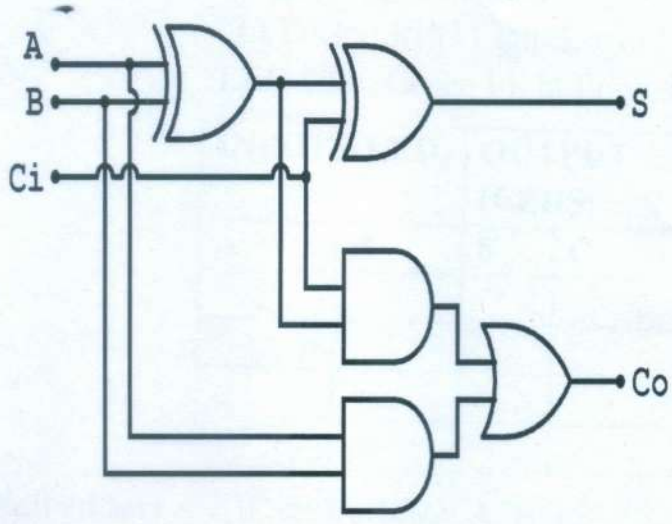
A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Truth Table

Boolean Expression: $S = A \oplus B$

$C = AB$

Full Adder: Full adder is a logical circuit that performs an addition operation on three binary digits. The full adder produces a sum and carries value, which are both binary digits. It can be combined with other full adders or work on its own.



Circuit Diagram of Full Adder

Input			Output	
A	B	Ci	S	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Truth Table

Boolean Expression: $S = A \oplus B \oplus Ci$

$$Co = AB + Ci(A \oplus B)$$

Procedure:

1. Collect the components necessary to accomplish this experiment.
2. Connect the inputs of the gate to the input switches of the LED.
3. Connect the output of the gate to the output LEDs.
4. Once all connections have been done, turn on the power switch
5. . Operate the switches and fill in the truth table (Write "1" if LED is ON and "0" if LED is OFF apply the various combinations of inputs according to the truth table and observe the condition of Output LEDs.

Observation Table:

Half Adder Input Variable: A, B
Output Variable: S, C
LED ON: RED Light:Logic 1
LED OFF: Green Light:Logic 0

INPUTS(LED)		**OUTPUT (LEDS)**	
A	**B**	**S**	**C**

Full adder: Input Variable: A, B, Ci
Output Variable: SUM(S), Carry (Co)
LED ON: RED Lioght:Logic 1
LED OFF: Green Light:Logic 0

INPUT(LED)			**OUTPUT(LED)**	
A	**B**	**Ci**	**Sum S**	**Carry Co**

Result:Verified the truth table as follows.